RESPONSE

Claims 1-23 were pending in the Application. Claims 1-23 stand rejected. Claims 1, 5, 6, 10, 11, 16, 17, 19, 20, and 22 are amended by the present Amendment. Support for the amendments may be found in the Specification at, for example, page 4, lines 10-11, and page 6, line 12 through page 7, line 13. Applicants respectfully submit that no new matter is introduced by the present Amendment. Upon entry of the present Amendment, claims 1-23 will be pending and presented for reconsideration.

Rejections Under 35 U.S.C. §112

Dependent claims 5, 2, 10, 11, 16, 19, and 22 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite. In particular, the Office Action suggests that the inclusion of the term "substantially" rendered claims 5, 2, 10, 11, 16, 19 and 22 indefinite because one of ordinary skill would not be able to ascertain "the requisite degree" from the specification. Because original claim 2 does not include the term "substantially", we presume that references to claim 2 in this section of the Office Action were intended to be references to claim 6 – the only other claim including the term "substantially" – and respond accordingly. Applicants have deleted the term "substantially" from claims 5, 6, 10, 11, 16, 19, and 22 thereby rendering the rejection moot. Applicants respectfully request reconsideration and withdrawal of the rejection of claims 5, 2 and/or 6, 10, 11, 16, 19, and 22 under 35 U.S.C. §112, second paragraph.

Rejections Under 35 U.S.C. §102

Claims 1-20 and 22-23 were rejected under 35 U.S.C. §102(e) as being unpatentable over U.S. Patent No. 6,457,073 to Barry (hereinafter "Barry").

Rejection of Independent Claim 1 Under 102(e) In View of Barry

Amended claim 1 is directed to a method for transferring portions of a memory block and

recites:

(a) configuring a first data mover with a first start address corresponding to a first portion of a source memory block;

(b) configuring a second data mover with a second start address corresponding to a second portion of the source memory block sized differently from the first portion;

(c) transferring, by the first data mover, the first portion of the source memory block at a first data rate; and

(d) transferring, by the second data mover, the second portion of the source memory block at a second data rate.

The Office Action suggests that Barry anticipates all of the elements of original claim 1. Claim 1 has been amended to further clarify Applicants' invention.

Generally, Barry teaches methods and apparatus for "initiating and controlling the sequence of data transfers; decoupling source and destination address generation through the use of independent specification of source and destination transfer descriptor." (Col. 2, lines 17-21). In particular, Barry teaches "a DMA controller implemented as a microprocessor consisting of multiple transfer controllers each supporting its own instruction thread." (Col. 2, lines 33-36).

Barry does not teach transferring data from the same memory block at different data rates. Barry instead teaches that "DMA instructions [are] typically of multi-word length and require a variable number of cycles to execute." (Col. 7, lines 22-24). Thus, as a clock cycle can be defined as "the time between two adjacent pulses of the oscillator that sets the tempo of the computer processor," (See www.whatis.com, definition of "clock cycle") Barry suggests only that each transfer controller may transfer data in a different amount of time. The "variable number of cycles" described in Barry can be cycles from the same oscillator of the computer processor. (See col. 7, lines 22-24). Barry does not, however, teach or suggest transferring data at different clock rates.

Amended claim 1 recites, in relevant part, "(c) transferring, by the first data mover, the first portion of the source memory block at a first data rate; and (d) transferring, by the second data mover, the second portion of the source memory block at a second data rate." As an example, the Specification teaches that, "[t]o enable the transfer of memory portions at different data transfer rates, the first D[ata]M[over] 8(a) may operate at a faster clock speed than the second D[ata]M[over] 8(b)." (Page 5, lines 5-7).

Since Barry does not teach or suggest transferring data at different clock rates, Barry does not teach or suggest all of the elements of amended independent claim 1. Thus, Applicants respectfully submit that amended independent claim 1 is patentable in view of Barry. Applicants further submit that these claims 2-16, which depend from independent claim 1 and include all of the limitations therein, are also patentable.

Rejection of Independent Claim 17 Under 102(e) In View of Barry

Amended claim 17 is a method for transferring portions of a memory block comprising the steps of:

(a) designating a master data mover;

(b) designating a slave data mover in communication with the master data mover;

(c) transmitting a start address to the master data mover, the start address identifying a first memory portion of a source memory block;

(d) transmitting the start address to the slave data mover to enable the slave data mover to determine a next address, the next address identifying a second memory portion of the source memory block sized differently from the first memory portion;

(e) transmitting a first write address identifying a first memory portion of a target memory block to the master data mover and a second write address identifying a second memory portion sized differently than the first memory portion of the target memory block to the slave data mover;

(f) transferring the first memory portion of the source memory block to the first write address identifying the first memory portion of the target memory block at a first data rate; and

(g) transferring the second memory portion of the source memory block to the second write address identifying the second memory portion of the target memory block at a second data rate.

The Office Action suggests that Barry anticipates all of the elements of claim 17. The Applicants respectfully traverse the rejection.

As discussed above with respect to claim 1, Barry does not teach or suggest transferring data at different clock rates. Thus, Barry does not teach or suggest "transferring the first memory portion of the source memory block to the first write address identifying the first memory portion of the target memory block at a first data rate," or "transferring the second memory portion of the source memory block to the second write address identifying the second memory portion of the target memory block at a second data rate," as recited in claim 17. Accordingly, Applicants respectfully submit that independent claim 17 is patentable over Barry. Applicants further submit that claims 18-19, which depend from independent claim 17 and incorporate all of the limitations therein, are also patentable over Barry.

Rejection of Independent Claim 20 Under 102(e) In View of Barry

Amended claim 20 is directed to a system to transfer portions of a memory block and recites:

(a) a first data mover;

(b) a second data mover in communication with the first data mover over a DM communications bus;

(c) a first memory component having a first portion and a second portion sized differently from the first portion and in communication with the first data mover and the second data mover over a first DM-memory bus; and

(d) a second memory component in communication with the first data mover and the second data mover over a second DM-memory bus,

wherein the first data mover transfers the first memory portion to the second memory component over the first DM-memory bus at a first data transfer rate, and

wherein the second data mover transfers the second memory portion to the second memory component over the second DM-memory bus at a second data transfer rate.

The Office Action suggests that Barry anticipates all of the elements of claim 20. The Applicants respectfully traverse the rejection.

As discussed above with respect to claim 1, Barry does not teach or suggest transferring data at different clock rates. Thus, Barry does not teach or suggest that the "first data mover transfers the first memory portion to the second memory component over the first DM-memory bus at a first data transfer rate," or that the "second data mover transfers the second memory portion to the second memory component over the second DM-memory bus at a second data transfer rate," as recited in claim 20. Accordingly, Applicants respectfully submit that independent claim 20 is patentable over Barry. Applicants further submit that claims 21-23, which depend from independent claim 20 and incorporate all of the limitations therein, are also patentable over Barry.

Priem Fails to Cure the Deficiencies of Barry

Claim 21 is rejected under 35 U.S.C. §103(a) as being unpatentable over Barry in view of U.S. Patent No. 6,457,073 to Priem et al. (hereinafter "Priem"). Applicants respectfully traverse the rejection.

Generally, Priem is a system and method for "accomplishing faster transfers of data directly from an application program to I/O devices." (Col. 2, lines 34-37). In particular, Priem teaches a new input/output architecture that can "drastically increase the speed of input/output operations for new application programs." (Col. 3, lines 25-30). Priem does not, however, teach

or suggest transferring data at two different data rates.

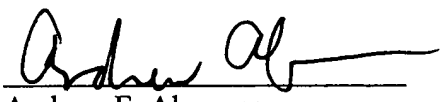
Thus, Priem and Barry, alone or in combination, fail to teach or suggest all of the elements of independent claims 1, 17, and 20. Accordingly, Applicants submit that these claims are patentable over Barry and Priem. Additionally, since claims 2-16, 18-19, and 21-23 depend from independent claims 1, 17, and 20, respectively, Applicants submit that these claims are also patentable.

SUMMARY

Claims 1-23 were pending in the Application. Claims 1-23 stand rejected. Claims 1, 5, 6, 10, 11, 16, 17, 19, 20, and 22 are amended by the present Amendment. Applicants request that the Examiner reconsider the application and claims 1-23 in light of the foregoing Amendment and Response, and respectfully submit that the claims, as amended, are in condition for allowance. If, in the Examiner's opinion, a telephonic interview would expedite the favorable prosecution of the present application, the undersigned attorney would welcome the opportunity to discuss any outstanding issues, and to work with the Examiner toward placing the application in condition for allowance.

A fee for submission of a Supplemental IDS under 37 C.F.R. §1.97(c) is also submitted herewith. Applicants believe that no additional fees are necessitated by the present Amendment. However, in the event that any additional fees are due, the Commissioner is hereby authorized to charge any such fees to Attorney's Deposit Account No. 20-0531.

Respectfully submitted,



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